PATENT SPECIFICATION (11) 1 560 270

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(21) Application No. 51767/77 (22) Filed 13 Dec. 1977
(44) Complete Specification published 6 Feb. 1980
(51) INT. CL.³ H03L 7/08
H04L 7/00
(52) Index at acceptance
H3A L2D1 L2M LX SL
H4P SX

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(54) IMPROVEMENTS IN OR RELATING TO DATA TRANSMISSION

(71) We, STANDARD TELEPHONES AND CABLES LIMITED, a British Company of 190 Strand, London W.C.2. England. do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:

This invention relates to data transmission, and especially to the derivation of a clock from the data as received at a data terminal.

A known method of transmission of a serial data stream to a remote terminal involves clocking the data at a line frequency several times higher than the data bit rate, and sending the redundantly-encoded signal to line via a modem. After demodulation at the receiving terminal, a running majority vote (hereinafter called RMV) performed on the n most recently-received line bits can provide basic error-correction, n being the nearest odd integer to the ratio of the line to data clock rates. The extraction of a data clock from this RMV signal enables the latter to be re-timed, so as to complete the error-correction.

We now refer to Fig. 1 of the drawings, which shows graphically the basic timing of such a system, with its error-correcting processes. Waveform (a) shows part of an asynchronous data stream to be transmitted, using non-return-to zero (NRZ) representations, while (b) shows the line clock, where frequency is, as can be seen, much higher than the data bit rate. With this frequency difference, adjacent data bits embrace numbers of clock periods which may differ by unity from each other. Waveform (c) shows the result of clocking waveforms (a) and (b) together, to give the data as sent to the line.

Waveform (d) shows the data of waveform (c) as received at a terminal: but with two line errors, A and B. The majority vote (RMV) is performed by counting, under the control of the line clock the relative numbers of 1 and 0 conditions in the received data stream for each set of n most recent line clock periods. In this case $n = 7$, so the majority vote $\frac{(n+1)}{2}$ is 4. As shown at (e), this causes error A, in the 1 condition period to be removed as shown dotted at A^1, while error B, as indicated at B^1, causes the transition at the end of the first 1 condition to be one line clock period late. Waveform (f) is the recovered data clock, and the present invention relates, as will be seen below, to the manner in which this clock is derived under the control of the received data stream.

Waveform (g) shows the RMV data of waveform (e) as it appears after a first retiming, and it will be seen that the delay in the transition which was caused by the line error B has been eliminated, as indicated at B^n. Finally at (h) we have the RMV data after its final retiming, and it will be seen that the normal alignment with the data clock has been restored, as indicated at C, (i.e. data transitions aligned with clock rising edges).

The object of the present invention is to provide an arrangement for deriving a data clock under the control of an incoming data signal, usable in a data transmission system.

According to the present invention, there is provided a clock pulse generation arrangement for use at a data received terminal, which includes a line clock pulse extraction system from which there is derived a data clock pulse train whose frequency is equal to the nominal bit rate of the data which the terminal receives, a transition detection circuit which monitors the incoming data stream for line condition transistions, comparison means adapted to

compare the timing of each said transition with the current data clock pulse phase, no action being taken if the transition occurs within a preset interval of time around the leading edge of the clock pulse, counting means under the control of the comparison means whose count is altered on each occasion at which a said transition is found to be outside said preset interval, the nature of count alteration depending on whether the transition is before or after the limits of said preset interval, and means responsive to the detection that the counting means, due to said alterations, has reached a limiting value (herein referred to as the shift threshold) to adjust the phase of the said data clock pulse train in a sense dependent on the direction in which the count has been altered to attain said shift threshold.

An embodiment of the invention will now be described with reference to the drawings, in which Fig. 2 is a simplified block diagram of as much of a data receiving terminal as is relevant to the invention, and Fig. 3 is a more detailed block diagram of the arrangement of Fig. 2.

As indicated above, the line clock frequency is not an integral multiple of the original data rate, so that some of the received data bits will embrace one more line bit than others. Further, although the data and line clock frequencies are nominally fixed, and hence should be synchronous relative to one another over a long period, they are in practice slightly asynchronous to one another due to tolerences on both of these frequencies. The system is intended to allow for both of these factors.

As the data is sent in a serial NRZ bit stream, the only data timing information received is in the line transitions. In such a system it is used to inject a synchronising preamble into the transmitted data stream whenever a consecutive stream of bits at the same logic level exceeds a specified time t. This is desirable because such a stream means that the line remains at one level for a relatively long period, and if no such action is taken, the receiver has no way to maintain synchronism. Thus the least amount of timing information conveyed to the receiver will come from a data transition rate of $1/t$.

Thus the system operates under the following conditions:

(a) line errors (to a specified limit)
(b) data bits of unequal length
(c) asynchronism between data and line frequencies (to a specified limit)
(d) as few as $1/t$ data transitions per second.

We now refer to Fig. 2, and here the line clock, whose frequency is a multiple of the bit rate (see Fig. 1) is applied to a phase-locked loop multiplier 1, which in turn feeds a clock divider 2, whose output is the recovered data clock, waveform (f) in Fig. 1. This has a frequency equal to the nominal bit rate, so that its frequency is lower than that of the line clock.

The received data is applied to a phase comparison circuit 3 to which the recovered data clock is also applied and this detects any differences between the line transition times and the times of the rising leading edges of the output of the clock divider 2. The result of this comparison is applied via a line error reduction block 4 to a phase shift control 5, which adjusts the phase of the pulses generated by the clock divider 2. As will be seen when we describe Fig. 3, a phase difference is ignored if it is less than a preset amount, which gives a "sync window" outside which a sync error is noted.

In addition to the control loop which includes blocks 3, 4, 5 there is a secondary control loop which varies the amount of information needed for this phase error detection in proportion to the amount of timing information received. This loop includes a timing logic block 6, which assesses from the number of transitions in the incoming information the amount of timing information in the data, and influences the phase shift control 5 via a phase error control block 7 in a manner appropriate to that amount.

Having given a very brief description of the arrangement for ensuring that the receiving terminal's data clock is adequately synchronised, we now turn to the more detailed block diagram shown in Fig. 3. Here the data, after it has been subjected to the majority vote referred to above is applied to transition detection logic 10, from which it is applied in the main control loop to a block 11, wherein synchronised data transitions are eliminated. This is achieved by virtue of the control of this block from the clock counter 12, which supplies the recovered data clock, via a sync window detection unit 13. This unit 13 is so controlled from the clock counter 12 as to block any data transitions which occur within the sync window. As already mentioned, this sync window is a period of time centered on a clock pulse rising leading edge, a data transition being accepted as valid if it occurs within that window period.

The output from the block 11 therefore consists of signals each of which corresponds to a data transition which occurs outside the sync-window. These signals are applied to a phase counter 14, this being the up-down counter referred to above. This block includes gating logic which is so controlled by the output of the clock

counter 12 that the phase counter is counted up or down dependant on the time relations between the data transistion on the line and the clock pulse rising edge. If the data transistion is early the counter in the block 14 is counted down by unity and if it is late the counter is counted up by unity.

The phase counter block 14 has two outputs, one of which goes to a −N detector 15 while the other goes to a +N detector 16. Each of these detects when the counter 14 has been subjected to N steps in one sense, which indicates that the phase shift threshold has been reached. Note that if a succession of mis-synchronised transitions were alternately before and after the sync-window, neither of these detectors would be able to respond. Whichever of these two detectors responds, a phase counter reset unit 17 is enabled, and the output of this unit when thus enabled resets the phase counter 14.

The clock counter 12 is normally driven from the line clock generator, via a phase-locked loop multipler 18, which produces an output whose frequency is a multiple of that of the line clock. The output of this block 18 is applied to a delay shift logic unit 19 where during correct operating conditions it is passed to the clock counter 12, which then functions as a divider to produce the recovered data clock.

If, due to the above operations the +N detector 16 gives an output, the delay shift logic 19 is enabled to inhibit a pre-set number of pulses in the signal from the multiplier 18 to the counter 12, thus introducing a phase delay to the counter 12, and in the recovered clock output. However, if the −N detector 15 responds, its output is effective via the advance shift logic unit 16A to cause the counter 12, to reset itself by a preset number of pulses earlier than would normally occur, which phase advances the counter 12 and the received clock outputs.

We now consider the secondary control loop, represented in Fig. 2 by the two blocks 6 and 7. To put this part of the system into a proper perspective, the main aspects of the system operation will be briefly recapitulated.

When a data transition is detected the current phase of the recovered clock is examined, and if the transition is within a short interval of time, the sync-window, centred on the clock rising leading edge, no action is taken as the clock is deemed to be in sync. However, when a transition is found to be outside the sync-window, the state of the up-down counter—the phase counter—is changed by unity. If the transition occurs during the high state of the recovered clock (i.e. it is late) the phase counter is incremented, and vice-versa. Thus if the clock and the data are out of sync, a net count gradually accummulates in the phase counter, the sign of the count indicating the direction of the phase error.

When the count in the phase counter reaches the shift threshold referred to above, the phase of the recovered clock is shifted by a fixed amount in a direction determined by the sign of the count. This is effected by the exertion of suitable control on the clock counter. In addition the phase counter is reset, and the cycle repeats if the shift has not yet reduced the phase error sufficiently.

Since a line error bit usually produces two erroneous transitions on the line, but only one after the RMV—see Fig. 1—the latter signal is used as the source of data timing information. A majority vote error is then typically a data transition which occurs one clock pulse period early or late. Such an error in otherwise synchronised data can be arranged to fall outside the sync window, and hence increment or decrement the phase counter. For random errors there should be about equal numbers of early and late transitions, so majority vote errors should tend to cancel each other in the phase counter, giving little net count. Thus the accuracy of the recovered clock is fairly independent of line errors.

Where, as in the waveform shown in Fig. 1, the line-to-data frequency ratio is not integral, some recovered data bits will embrace more line clock bits than others. The sync window is not usually wide enough to accommodate both bit lengths, which will produce some clocking of the phase counter. In practice the system finds an equilibrium when equal numbers of transitions fall before and after the sync window.

Data/line clock asynchronism due to clock tolerances may produce a gradual phase drift between data and recovered clock. When the phase drift thus produced is enough the phase counter induces a shift in the recovered clock to improve sync. Thus the clock can remain locked to the asynchronous data.

The requirements for the optimum shift threshold tend to conflict: this is resolved by allowing this to be a variable parameter controlled between limits N_{MIN} and N_{MAX} by the transition rate. This threshold is set equal to the number of transitions arriving in time t, subject to the limits indicated above. Thus the shift threshold is normally updated at intervals of t, with the exception that if N_{MAX} transitions have been received before the expiry of the period t, the threshold is up-dated to N_{MAX} and the count and t both restarted.

At this point we revert to Fig. 3, where the transistor detection logic 10 has a

second output which goes to transition rate logic 20, this connection being direct and not via the elimination circuit 11.

The transistion rate logic 20 is a counter which totalizes the number of line transitions received since its last reset. This total count is applied to the shift threshold latch 22 and to a control block 21. This block 21 derives a timing pulse t from the line clock, and also examines the output of the transition rate logic for the limit count N_{MAX}.

When either t or N_{MAX} is reached, block 21 latches the current output of the transition rate logic 20 into the shift threshold latch 22, and resets itself and the counter in the transition rate logic 20. The output of the latch 22 now holds an updated value of $+N$, and will be held until t or N_{MAX} is again detected by clock 21. A valve for $-N$ is obtained from a complementer 23.

Allowing the shift threshold to be a dynamic quantity determined by the secondary control loop assists in meeting system performance requirements.

Thus for low transition rates a low value of shift threshold enables the system to maintain its phase lock to asynchronous data, and at higher transition rates a larger threshold permits effective error cancellation.

To complete the error correction process, the falling edge of the recovered clock retimes the majoriay vote data in the middle of each data bit, since this is the point in a majority vote bit which is least likely to be corrupted by line errors. Finally the data can be retimed again by the rising edge of the recovered clock, which restores normal alignment. With all received data bits now of equal length, aligned to clock, and most errors corrected, the data stream can be routed to its final destination.

Negligible output errors are produced by data/clock phase errors, so improvements in the clock recovery system do not affect output error rate. Improvements are possible, however, in the area of clock jitter in certain cases. Thus as the value of N can be controlled by the transition rate to optimise error immunity so that shift distance could be varied, in one of two ways.

In the first of these two ways, when the transition rate exceeds that needed for N_{MAX}, we have a shift rate capability which exceeds that needed to overcome the specified asynchronism. Instead of allowing a greater maxium asynchronism, as done in the arrangements described above, we can allow the shift distance to be reduced. This may offset the increased shift rate capability so the maximum permitted value A_{MAX} of the asynchronism between the data clock rate and the line clock rate is unchanged.

In the second of these two ways, instead of incrementing the phase counter by unity for any transition which falls outside the sync window, means is provided to record the approximate magnitude of the phase error. This is done by using extra phase counters and more complex sync window logic. Each unsynchronised transition is steered to the phase counter for the appropriate band of phase error. The shift distance produced in a phase counter reaching $\pm N$ varies, such that counters associated with greater phase errors bands are shifted by greater amounts, and vice versa.

The second of these two is the more comprehensive as the jitter reduction would work for all data transition rates, but may be difficult to implement or optimise. The first of these two has the merit of simplicity in analysis and optimisation, and as usually one only needs a low data transition rate for N to reach N_{MAX}, its operation only for transition rates above this level is not a great advantage.

WHAT WE CLAIM IS:

1. A clock pulse generation arrangement for use at a data receiving terminal, which includes a line clock pulse extraction system from which there is derived a data clock pulse train whose frequency is equal to the nominal bit rate of the data which the terminal receives, a transition detection circuit which monitors the incoming data stream for line condition transitions, comparison means adapted to compare the timing of each said transition with the current data clock pulse phase, no action being taken if the transition occurs within a preset interval of time around the leading edge of the clock pulse, counting means under the control of the comparison means whose count is altered on each occasion at which a said transition is found to be outside said preset interval, the nature of the count alteration depending on whether the transition is before or after the limits of said preset interval, and means responsive to the detection that the counting means, due to said alterations, has reached a limiting value (hereinafter referred to as the shift threshold) to adjust the phase of the said data clock pulse train in a sense dependent on the direction in which the count has been altered to attain said shift threshold.

2. An arrangement as claimed in claim 1, and in which the counting means is a single up-down counter whose count is altered by one step each time a said transition is found to be outside said preset interval.

3. An arrangement as claimed in claim 1, in which the counting means includes a set of counters each of which is appropriate to an error of a different magnitude and direction, and in which means under control of said comparison means assesses

the extent of an error and, under control of said assessment, selects the appropriate one of said counters, so that the shift distance which is produced in different ones of said counters to reach said threshold varies.

4. An arrangement as claimed in claim 1, 2 or 3, in which the output of said transition detection circuit is applied to a synchronised transition eliminator, which ensures that transitions regarded as being in synchronism with the data clock are not applied to said comparison means, and in which said eliminator is controlled from the data clock via a window detection circuit which causes said eliminator to block the passage of signals which represent transitions which occur within said window.

5. An arrangement as claimed in claim 2 or claim 3 with claim 2 in which said up-down counter has two outputs which go respectively to positive (+N) and negative (−N) shift threshold detectors forming said detection-responsive means, one of said detectors responding when said shift threshold is attained, and in which said response, in addition to effecting said adjustment of the clock phase, also resets said up-down counter to its rest condition.

6. An arrangement as claimed in claim 5, in which the clock whose phase is to be controlled is derived from an intermediate clock pulse source whose frequency is high compared with that of the bit rate, said source being divided by a counter acting as a frequency divider to produce the clock whose phase is to be controlled, in which the output source is applied to the counter via delay shift logic which is enabled to inhibit a preset number of pulses in response to an output from said +N detector, thereby making the required phase adjustment, and in which when said −N detector gives an output it enables advance shift logic to reset said counter a preset number of pulses earlier then usual to make the required phase adjustment.

7. An arrangement as claimed in claim 6, and in which said line clock feeds a phase-locked loop multiplier the output of which is said intermediate clock pulse train which is applied to said delay shift logic.

8. An arrangement as claimed in claim 5 or in any claim appendant thereto, in which the line data is conveyed in a non-return to zero representations, and in which the shift threshold is adjustable between minimum and maximum values N_{MIN} and N_{MAX} under control of the transistion rate of the line data.

9. A clock pulse generation arrangement, substantially as described with reference to the accompanying drawings.

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Printed for Her Majesty's Stationery Office by The Tweeddale Press Ltd., Berwick-upon-Tweed, 1980.
Published at the Patent Office, 25 Southampton Buildings, London, WC2A 1AY, from which copies may be obtained.

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2 SHEETS *This drawing is a reproduction of the Original on a reduced scale*
Sheet 1

Fig.1.

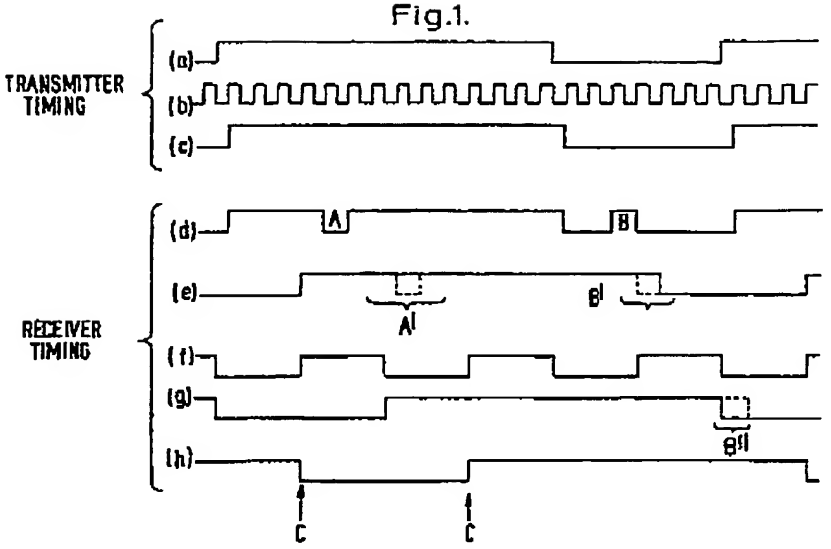
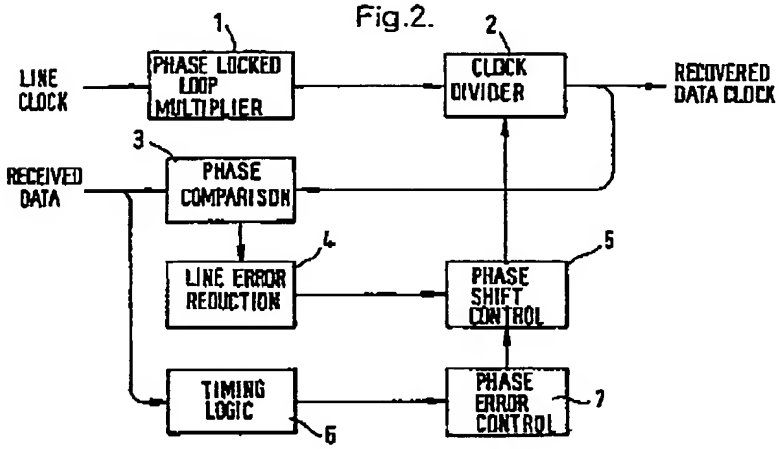


Fig.2.



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Sheet 2

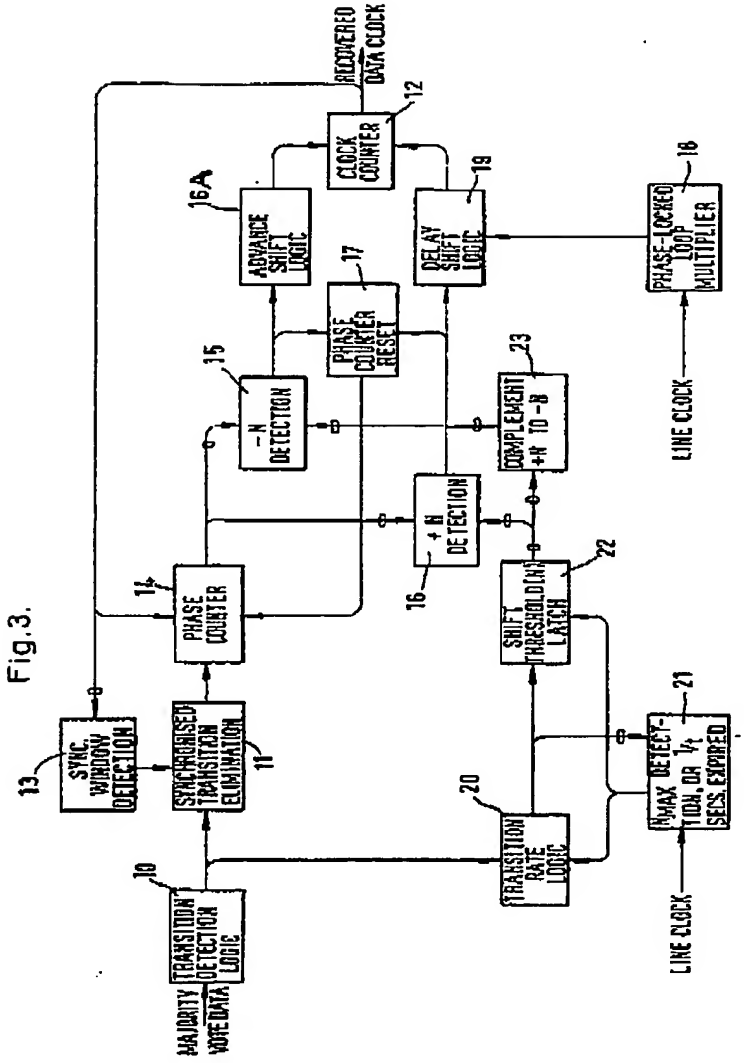

Fig.3.